WHAT IS CLAIMED

1. A method for direct access to bit fields in instruction operands, the method comprising:

providing a bit field consisting of a plurality of bits in a plurality of bit positions;

performing instruction operations utilizing bit fields in source and target operands; and

providing direct manipulation of any bits in any bit field.

2. The method for direct access to bit fields in instruction operands according to claim 1, further comprising:

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator;

wherein no instruction depends on a preceding instruction because each instruction in a pipeline is executed for a different thread.

3. The method for direct access to bit fields in instruction operands according to claim 1, further comprising:

transferring the data after modifying and forwarding to an output buffer.

4. The method for direct access to bit fields in instruction operands according to claim 1, further comprising:

processing data at a rate of at least 10 Gbs.

5. An apparatus for directly accessing bit fields in instruction operands, said apparatus comprising;

at least one memory;

at least one processor;

a bus interconnecting said at least one memory and said at least one processor;

wherein one of said at least one processor retrieves a bit field consisting of a plurality of bits in a plurality of bit positions, performs instruction operations utilizing bit fields in source and target operands, and provides direct manipulation of any bits in any bit field.

6. The apparatus for directly accessing bit fields in instruction operands according to claim 5, wherein said processor comprises:

an analysis machine having multiple pipelines;

a packet task manager operationally connected to said analysis machine; and,

a packet manipulator operationally connected to said analysis machine.

7. The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

8. The apparatus according to claim 6, wherein said analysis machine has 32 threads.

9. The apparatus according to claim 6, further comprising:

a packet task manager operationally connected to said analysis machine; and

a packet manipulator operationally connected to said analysis machine

a global access bus including a master request bus and a slave request bus separated from each other and pipelined.

10. The apparatus according to claim 6, further comprising:

an external memory engine operationally connected to said analysis machine; and

a hash engine operationally connected to said analysis machine.

11. The apparatus according to claim 9, further comprising:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine.

12. The apparatus according to claim 9, further comprising:

packet data global access bus software code used for flow of packet data between a flexible data input bus and a packet manipulator.

13. The apparatus according to claim 9, further comprising:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator.

14. The apparatus according to claim 9, further comprising:

private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

15. The apparatus according to claim 9, further comprising:

lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

16. The apparatus according to claim 9, further comprising:

results global access bus software code used for providing flexible access to an external memory.

17. The apparatus according to claim 9, further comprising:

results global access bus software code used for providing flexible access to an external memory.

18. The apparatus according to claim 9, further comprising:

a bi-directional access port operationally connected to said analysis machine;

a flexible data input buffer operationally connected to said analysis machine; and

a flexible data output buffer operationally connected to said analysis machine.